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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/183,389	10/29/1998	VLADIMIR BEREZIN	08305/048001	3070

7590 08/25/2005

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EXAMINER	
WHIPKEY, JASON T	

ART UNIT	PAPER NUMBER
2612	

DATE MAILED: 08/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/183,389	BEREZIN, VLADIMIR	
	Examiner	Art Unit	
	Jason T. Whipkey	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see pages 3-4, filed November 24, 2004, with respect to the rejections of claims 9-26 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground of rejection is made in view of Morris and Yadid-Pecht.

2. Because a new ground of rejection is being applied to unamended claims, this action is non-final.

Drawings

3. The proposed drawing correction filed July 1, 2004, is approved. *In order to avoid abandonment, the drawings must now be corrected.*

The proposed drawing correction practice was eliminated effective July 30, 2003. See 68 Fed. Reg. 38,611, 38,629 (June 30, 2003) (codified at 37 C.F.R. pt. 1.121(d)).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 9, 10, 12, 13, and 15-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morris (U.S. Patent Application Publication No. 2003/0058345) in view of Yadid-Pecht (U.S. Patent No. 6,115,065).

Regarding **claims 9, 18, and 21**, Morris discloses an imaging system (see Figure 5), comprising:

an active pixel sensor array (sensor sub-array 510; see paragraphs 27 and 14) disposed on a substrate (all components are located on a common chip; see paragraph 35), said array comprising a plurality of pixels (see paragraph 27);

at least one analog to digital converter (520) for sampling and converting analog information from pixels in said array to digital values (see paragraph 27); and

a plurality of digital memory arrays (register files 530 and 550; see paragraph 27) disposed on said substrate (see paragraph 35) for storing said digital values (see paragraph 28).

Morris is silent with regard to sampling each pixel multiple times during an integration period and storing each sampled value.

Yadid-Pecht discloses an image sensor, wherein:

> each pixel in said active pixel image sensor array is sampled[1] multiple times during an integration period (multiple readings are taken from each pixel to complete a frame; see column 5, lines 18-50) and each sampled value is stored in one of said memory arrays (signal chains 204 and 206; see column 4, lines 53-58).

As stated in column 3, lines 35-37, an advantage of sampling each pixel multiple times during an integration period and storing each value is that the sensor's dynamic range may be increased. For this reason, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Morris's imaging device sample each pixel multiple times during an integration period.

Regarding **claims 10 and 19**, it is inherent that the active pixel image sensor array disclosed by Morris is a CMOS image sensor.

Regarding **claim 12**, Morris is silent with regard to including column analog double sampling circuitry.

Yadid-Pecht discloses:

> an analog signal processor including column analog double sampling circuitry (see column 7, lines 34-38).

As stated in column 7, lines 34-38, an advantage of performing CDS is that noise can be suppressed. For this reason, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Morris's imaging device perform CDS.

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[1] The examiner notes the disparity between Applicant's terminology and the terminology used by Yadid-Pecht. In the instant application, a plurality of samples are taken, which, in aggregate, form a single integration, equivalent to a frame (see page 4, lines 15-21, of the specification). Yadid-Pecht performs a plurality of integrations, which, in aggregate, form a single frame. In other words, Applicant's sample is equivalent to the reference's integration, and Applicant's integration is equivalent to the reference's frame.

Regarding **claim 13**, the double sampling circuitry disclosed by Yadid-Pecht inherently samples both a signal and a reference for decreasing pixel fixed pattern noise.

Regarding **claim 15**, Morris discloses:

> said at least one analog to digital converter (520) comprises a column analog to digital converter for each pixel column (see paragraphs 27 and 16) of said active pixel image sensor array.

Regarding **claim 16**, both Morris and Yadid-Pecht are silent with regard to including a digital signal processor between the A/D converter and one of the digital memory arrays.

Official Notice is taken that digital signal processing is commonly performed on pixel data before it is stored in memory. An advantage of performing DSP is that image quality may be improved. For this reason, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Morris include a digital signal processor between the A/D converters and the memories.

Regarding **claims 17**, Yadid-Pecht discloses:

> stored multiple sampled digital values for each pixel stored in said one of said plurality of digital memory arrays are used to provide an integrated output signal for each pixel (see column 5, lines 18-50).

Regarding **claim 20**, Yadid-Pecht discloses:

> using the stored digital values for each pixel to produce a respective integrated pixel output signal for said integration period (see column 5, lines 18-50).

Regarding **claim 22**, Morris discloses:

said plurality of digital memory arrays comprises two digital memory arrays (see Figure 5).

Regarding **claim 23**, Morris is silent with regard to disposing the two digital memory arrays on opposite sides of the image sensor array. However, the courts have held that that mere rearrangement of parts is obvious. See In re Japikse, 86 USPQ 70 (CCPA 1950).

Consequently, it would have been obvious to one of ordinary skill in the art at the time the invention was made to arrange the digital memories in any configuration, including on opposite sides of the image sensor array.

Regarding **claim 24**, Yadid-Pecht discloses:

integrating said first and second pluralities of values to produce a first integrated value and a second integrated value respectively (see column 5, lines 18-50).

Regarding **claim 25**, Morris is silent with regard to disposing the two digital memory arrays on opposite sides of the image sensor array. However, the courts have held that that mere rearrangement of parts is obvious. See In re Japikse, 86 USPQ 70 (CCPA 1950).

Consequently, it would have been obvious to one of ordinary skill in the art at the time the invention was made to arrange the digital memories in any configuration, including on opposite sides of the image sensor array.

Regarding **claim 26**, Morris is silent with regard to performing analog and digital signal processing.

Yadid-Pecht discloses:

an analog signal processor (CDS circuitry; see column 7, lines 34-38) coupled to at least one pixel of said plurality of pixels of said active pixel sensor array.

As stated in column 7, lines 34-38, an advantage of performing analog signal processing is that noise can be suppressed. For this reason, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Morris's imaging device perform analog signal processing.

Yadid-Pecht is silent with regard to including a digital signal processor.

Official Notice is taken that digital signal processing is commonly performed on pixel data before it is stored in memory. An advantage of performing DSP is that image quality may be improved. For this reason, it would have been obvious at the time of invention to have Morris include a digital signal processor.

6. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Morris in view of Yadid-Pecht and further in view of Mandl (U.S. Patent No. 5,248,971).

Claim 11 may be treated like claim 9. However, Morris is silent with regard to the A/D converters being oversampling converters.

Mandl shows in Figures 3A and 3B a video camera that uses an oversampling A/D converter (column 4, line 67 through column 5, line 3). A/D converter 144 in Figure 3B digitizes charges from array column 156 (column 5, line 67 through column 6, line 16). The charges from array column 156 are oversampled (column 6, lines 50-56).

As stated in column 10, lines 14-20, an oversampling A/D converter in an imaging system improves image quality. For this reason, it would have been obvious to have Morris's system utilize an oversampling A/D converter.

7. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Morris in view of Yadid-Pecht and further in view of Lee (U.S. Patent No. 6,466,265).

Claim 14 may be treated like claim 12. However, Morris is silent with regard to including a preamplifier with adjustable gain.

Lee discloses an active pixel sensor (see Figure 2e):

> said analog signal processor further comprises at least one preamplifier (programmable gain amplifier 93; see column 5, lines 23-25) with adjustable gain (via a variable gain element; see column 5, lines 52-54).

An advantage of using a variable gain amplifier is that the gain of the pixel signals may be adjusted to reach a uniform value based on lighting conditions. For this reason, it would have been obvious at the time of invention to have Morris's image sensor include a variable gain amplifier.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Whipkey, whose telephone number is (571) 272-7321. The examiner can normally be reached Monday through Friday from 9:00 A.M. to 5:30 P.M. eastern daylight time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thai Tran, can be reached at (571) 272-7382. The fax phone number for the organization where this application is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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August 12, 2005